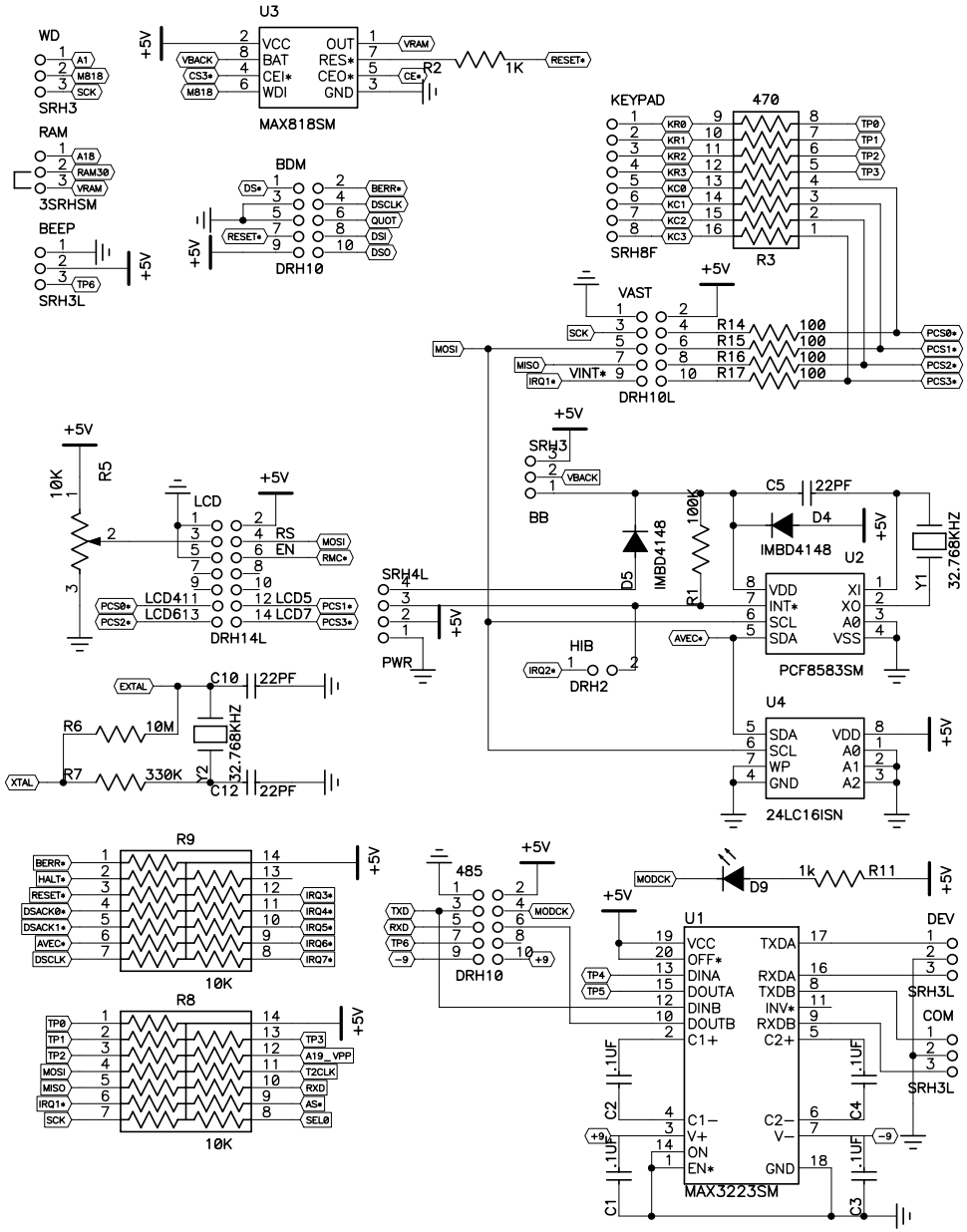

Port E		Port F		TPU I/O	CSB Boot ROM
DACK0	bus	MODCK	T/R*,LED	TP0 KC0	CS0 RAM WRH*
DACK1	bus	IRQ1*	VINT*	TP1 KC1	CS1 RAM WRL*
AVEC	SDA	IRQ2*	IRQ2* RTC	TP2 KC2	CS2 RAM OE*
RMC	ENLCD*	IRQ3*	bus	TP3 KC3	CS3 RAM CE*
DS*	funct	IRQ4*	bus	TP4 TxDB	CS4 Bus memory
AS*	funct	IRQ5*	bus	TP5 RxDB	CS5 Bus I/O
SIZ0	bus	IRQ6*	BINT* bus	TP6 BEEP, 16X	CS6 A19
SIZ1	bus	IRQ7*	NMI* bus	TP7–15, bus	CS7 A20
					CS8 A21
					CS9 A22
					CS10 Flash CS*

Rev 1.1
PAL connect to SEL0 and jumper to GND, SEL0 and AS* connected to R8
Diodes, RC added between MISO and VAST, PWR connector per standard

Rev 1.2
Added series resistors to VASTaddr outputs
Added LED to MODCK, Routed TP0–3 to J2D
Added IRQ2* disconnect jumper

Rev 1.3
Added fudicials for auto insertion equipment, moved caps from edge, renumbered ICs

The information contained in this document is not intended as a guide to the design of a 68332 microprocessor based product.

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